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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/747,946	12/31/2003	Joon Bum Shim	040008-0305451	6221

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EXAMINER	
NGUYEN, THANH T	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/747,946	SHIM ET AL.	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *13-19 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *13-19 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Request for Continued Examination

The request filed on 11/26/06 for a Request for Continued Examination (RCE) under 37 CFR 1.114 is acceptable and an RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13-14, 17, 19, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (U.S. Patent No. 6,878,646) in view of Mori (U.S. Patent No. 2004/0038436) and Wolf "silicon processing for the VLSI ERA" vol. 2, page 194, pages 542-551.

Referring to figures 2a-2g, Tsai teaches a method of fabricating a submicron semiconductor device comprising:

Forming an oxide layer (100) on a substrate (80);

Forming a polysilicon layer (110) on the oxide layer;

Forming a hardmask (120) on the polysilicon layer;

Depositing a photoresist (140) on the hardmask and patterning the photoresist by using a mask (see figure 1B);

Etching the hard mask (120) by plasma etching (see figure 1D, col. 5, lines 21-30) to form a thin hard mask pattern by using the photoresist pattern as an etching mask so that the hard mask pattern can have a narrower width than that of the photoresist pattern (see figure 1D);

Etching the polysilicon layer (110) by using the hard mask pattern (120) as an etching mask to form a gate electrode in the polysilicon layer having a desired critical dimension smaller than a corresponding critical dimension in the hard mask (see figures 1F-1G); and

Wherein the hard mask (120) has a thickness of about 150-400 A^{o} (see col. 4, lines 41-45).

Regarding to claims 14, depositing an ARC (130) the hard mask (120) so as to lower reflectivity (figure 1A).

Regarding to claims 15, 17, wet etching to remove the hard mask pattern is performed at the temperature of $50\text{-}130^{0}$ (see col. 6, lines 30-67, col. 7, lines 35-56).

However, Tsai et al. does not teach forming a thermal oxide layer on a substrate, etching a polymer formed as a residual product resulting from etching the polysilicon layer by using HF solution, depositing oxide layer by using SiH_4 oxide in PECVD process, pattern the photoresist by using KrF laser as a light source, removing the hard mask layer by wet etching using HF gas and nitrogen gas, the percentage of HF, the temperature, and etching rate of the hard mask layer

Mori et al. teaches forming a thermal oxide (204, see paragraph# 51), forming a polysilicon (203) on the oxide, forming a hardmask layer (208) on the polysilicon, forming an ARC layer (202), forming a photoresist pattern (201) on the ARC layer (see figure 2a) by using

KrF laser as a light source (see paragraphs# 8, 14, 71), etching the hard mask layer by using plasma etch (see paragraph# 49, etching the polysilicon layer by using plasma etch using $Cl_2/SF_6/O_2$ (see paragraphs# 50-52), etching a polymer formed as a residual product resulting from etching the polysilicon layer by using HF solution (see paragraphs# 54). Noted that since the cleaning solution by using HF, it would inherent remove any polymers contaminant.

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etching the polysilicon layer by using plasma etch using $Cl_2/SF_6/O_2$, remove a polymer formed as a residual product resulting from etching the polysilicon layer by using HF solution, pattern the photoresist by using KrF laser as a light source in process of Tsai et al. to form a gate structure as taught by Mori et al. because the process would remove undesired residual on the gate to form a gate structure a desire a gate structure with low cost.

Wolf teaches forming the oxide layer by using silane (SiH_4 gas) and O_2 to form a silane-oxide layer by PECVD method (see table 4, page 194 of Wolf) and etching the oxide hardmask layer by using plasma SF_6 (see pages 542-551, table 2).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would from the silane-oxide layer by PECVD, etching the oxide hardmask layer by using plasma SF_6 in process of Tsai et al. as taught by Wolf because forming the PECVD oxide layer by using silane gas is known in the art to provide a good step coverage, etching the oxide hardmask layer by using plasma SF_6 to provide high selectivity.

Claims 15-16, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai et al. (U.S. Patent No. 6,878,646) in view of Mori (U.S. Patent No. 2004/0038436) and Wolf

"silicon processing for the VLSI ERA" vol. 2, page 194, pages 542-551, and Bergman (U.S. Patent No. 5332445).

Tsai et al in view of Mori teaches forming the hard mask film and etching the hard mask film with HF. However, the references do not teach removing the hard mask layer by wet etching using HF gas and nitrogen gas, the percentage of HF, the temperature, and etching rate of the hard mask layer.

Bergman teaches etching the hardmask (oxide/nitride) layer by using HF and nitrogen gas (see col. 3, lines 41+, and col. 6, lines 15+).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time of the invention was made would etch the hardmask (oxide/nitride) layer by using HF and nitrogen gas in process of Tsai et al. as taught by Bergman because the process would provide high speed etching of good uniformity and superior particle count performance.

The etching rate, the percentage of HF, the temperature, etching selectivity, and the thickness of the hardmask layer range of claims 6, 12, 15-18 are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller, the selection of reaction parameters such as temperature and concentration would have been obvious:

> Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed □critical ranges and the applicant has the burden of proving such criticality.... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.□
> *In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA*

1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Therefore, one of ordinary skill in the requisite art at the time the invention was made would have used any etching rate, the percentage of HF, the temperature, etching selectivity, and the thickness range suitable to the method in process of Tsai et al. because the process would provide a desirable gate with high etching selectivity and low cost.

Response to Arguments

Applicant's arguments filed 1/26/06 have been fully considered but they are not persuasive.

Applicant contends, Tsai et al. do not disclose or suggest a thermal oxide film, forming a hard mask SiH_4 oxide by PECVD. In response to applicant, Tsai et al. do not disclose or suggest a thermal oxide film, forming a hard mask SiH_4 oxide by PECVD. However, Mori et al. clearly teach forming a thermal oxide film (204, see paragraph# 51). Wolf et al. clearly teach forming the SiH_4 oxide by PECVD (see table 4, page 194 of Wolf). It is noted that it is known SiH_4 oxide formed by PECVD means that SiH_4 react with any form of oxygen containing gas to form oxide by using PECVD, unless there is some other way to form silane oxide which applicant disclosed in the specification that examiner had not seen.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN